

What Is Claimed Is:

1 1. A method of forming a memory cell with a single sided
2 buried strap, comprising the steps of:
3 providing a substrate having a trench;
4 forming a trench capacitor at a lower portion of the trench;
5 forming a collar insulating layer on a sidewall of an upper
6 portion of the trench;
7 forming a first conductive layer above the trench capacitor
8 and filling the trench;
9 removing part of the first conductive layer and part of the
10 collar insulating layer to form a remaining first
11 conductive layer and a remaining collar insulating
12 layer in an opening, wherein the opening has a first
13 sidewall and a second sidewall, and a top surface of
14 the remaining collar insulating layer is lower than
15 that of the remaining first conductive layer;
16 performing an angle implantation with fluorine-containing
17 ions on the first sidewall of the opening;
18 performing a thermal oxidation process to form a first
19 oxide layer on the first sidewall and a second oxide
20 layer on the second sidewall, wherein a thickness of
21 the first oxide layer is greater than that of the
22 second oxide layer;
23 removing the second oxide layer to expose the second
24 sidewall; and
25 forming a second conductive layer serving as a buried strap
26 at a bottom of the opening, wherein the second
27 conductive layer is insulated from the first sidewall
28 by the first oxide layer.

1 2. The method according to claim 1, further comprising
2 the steps of:
3 forming an insulating layer on the second conductive layer;
4 forming a gate insulating layer on the second sidewall;
5 forming a gate in the opening; and
6 forming a source region and a drain region in the substrate.

1 3. The method according to claim 1, wherein the formation
2 of the trench comprises the steps of:
3 forming a patterned pad layer on the substrate; and
4 using the pad layer as a mask, removing part of the
5 substrate to form a trench in the substrate.

1 4. The method according to claim 1, wherein the substrate
2 is a silicon substrate.

1 5. The method according to claim 3, wherein the pad layer
2 comprises an oxide pad layer and a nitride layer.

1 6. The method according to claim 1, wherein the collar
2 insulating layer is a SiO₂ layer.

1 7. The method according to claim 1, wherein the first
2 conductive layer is a doped polysilicon layer.

1 8. The method according to claim 1, wherein the
2 fluorine-containing ions comprise F and/or BF₂ ions.

1 9. The method according to claim 1, wherein an
2 implantation energy of the angle implantation is 15~30keV.

1 10. The method according to claim 9, wherein a dosage of
2 the angle implantation is 1E14~4.5E15 ions/cm².

1 11. The method according to claim 1, wherein an operating
2 temperature of the thermal oxidation process is 900~950°C.

1 12. The method according to claim 1, wherein the second
2 conductive layer is a doped polysilicon layer.

1 13. The method according to claim 2, wherein the gate
2 oxide layer is a SiO₂ layer formed by thermal oxidation.

1 14. The method according to claim 13, wherein an operating
2 temperature of the thermal oxidation process is 800~1000°C.

1 15. A method of forming a memory cell with a single sided
2 buried strap, comprising the steps of:

3 providing a substrate;

4 forming a patterned pad layer on the substrate;

5 using the pad layer as a mask, removing part of the
6 substrate to form a trench therein;

7 forming a trench capacitor at a lower portion of the trench;

8 forming a collar insulating layer on a sidewall of an upper
9 portion of the trench;

10 forming a first conductive layer above the trench capacitor
11 and filling the trench;

12 removing part of the first conductive layer to a determined
13 depth, thus forming a remaining first conductive
14 layer;

15 removing part of the collar insulating layer to form a
16 remaining collar insulating layer in an opening,
17 wherein the opening has a first sidewall and a second
18 sidewall, and a top surface of the remaining collar

19 insulating layer is lower than that of the remaining
20 first conductive layer;
21 performing an angle implantation with fluorine-containing
22 ions on the first sidewall of the opening;
23 performing a thermal oxidation process to form a first
24 oxide layer on the first sidewall and a second oxide
25 layer on the second sidewall, wherein a thickness of
26 the first oxide layer is greater than that of the
27 second oxide layer;
28 removing the second oxide layer to expose the second
29 sidewall; and
30 forming a second conductive layer serving as a buried strap
31 at a bottom of the opening, wherein the second
32 conductive layer is insulated from the first sidewall
33 by the first oxide layer;
34 forming an insulating layer on the second conductive layer;
35 forming a gate insulating layer on the second sidewall;
36 forming a third conductive layer serving as a gate in part
37 of the opening;
38 forming an insulating spacer on the sidewall of the
39 opening;
40 forming a fourth conductive layer to fill the opening;
41 forming a fifth conductive layer on the fourth conductive
42 layer; and
43 forming a source region and a drain region in the substrate.

1 16. The method according to claim 15, wherein the
2 substrate is a silicon substrate.

1 17. The method according to claim 15, wherein the
2 fluorine-containing ions comprise F and/or BF₂ ions.

1 18. The method according to claim 15, wherein an
2 implantation energy of the angle implantation is 15~30keV and
3 a dosage of the angle implantation is $1E14 \sim 4.5E15$ ions/cm².

1 19. The method according to claim 15, wherein an operating
2 temperature of the thermal oxidation process is 900~950°C.

1 20. The method according to claim 15, wherein the gate
2 oxide layer is a SiO₂ layer formed by thermal oxidation.